**Listing of the Claims:**

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Currently Amended) An electronic circuit for cryptographic processing, ~~having a set of combinatorial logical circuits, the set of combinatorial logical circuits~~ comprising:

a first combinatorial logical circuit, having an input, arranged to perform a first set of logical operations on input data at the input and to produce a corresponding output data, the output data having a given functional relation to the input data, and ~~characterized in that the set of combinatorial logical circuits further comprises at least~~

a second combinatorial logical circuit, having an input, arranged to perform a second set of logical operations on ~~the same~~ input data at said input and to produce output data, the output data having a ~~an identical~~ functional relation to the input data identical to the given functional relation,

wherein the first set of logical operations is different from the second set of logical operations, and

a selector for receiving a given input data and ~~wherein the electronic circuit is arranged to~~ dynamically selecting from among the first ~~one~~ combinatorial logical circuit and the second combinatorial logical circuit ~~of the~~

set of combinatorial logical circuits for performing logical operations on the given the input data and producing output data, and

wherein the selecting includes inputting the given input data to the input of the selected one of the first and second combinatorial logical circuits and outputting a selected output, the selected output being the output of the selected one of the first and second combinatorial logical circuits.

2. ( Currently Amended) The electronic circuit according to claim 1, further comprising:

a third combinatorial logical circuit, having an input, arranged to perform a third set of logical operations on input data at the input and to produce a corresponding output data, the output data having a given functional relation to the input data, and

a fourth combinatorial logical circuit, having an input, arranged to perform a fourth set of logical operations on input data at said input and to produce output data, the output data having a functional relation to the input data identical to said given functional relation,

wherein the third set of logical operations is different from the fourth set of logical operations, and

a selector for receiving said selected output data and dynamically selecting from among the third combinatorial logical circuit and the fourth

combinatorial logical circuit for performing logical operations on the selected output data and producing a second output data, and

wherein said selecting includes inputting the selected output data to the input of the selected one of the third and fourth combinatorial logical circuits ~~comprising at least a first set of combinatorial logical circuits and a second set of combinatorial logical circuits, and arranged to use output data produced by the first set of combinatorial logical circuits as input data of the second set of combinatorial logical circuits~~.

3. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 1, wherein the selector comprises ~~further comprising~~:

[[-]] a selection circuit ~~arranged~~ for generating a signal to select one combinatorial logical circuit of the set of combinatorial logical circuits,

[[-]] a splitter circuit ~~arranged~~ for inputting the given input data to one of the first and second combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits, depending on the signal,

[[-]] a merger circuit ~~arranged~~ for outputting data from one of the first and second combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits, depending on the signal.

4. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 3, further comprising a timing circuit ~~arranged~~ to determine the points in time at which the selection circuit generates the signal to select one of the

first and second combinatorial logical combinatorial logical ~~circuit of the set of combinatorial logical~~ circuits.

5. (Currently Amended) An electronic circuit for cryptographic processing, comprising:

[[-]] a combinatorial logical circuit ~~arranged~~ to perform logical operations on input data and to produce an output data,

[[-]] a storage circuit ~~element~~ for storing the output data produced by the combinatorial logical circuit, ~~characterized in that~~

wherein the storage ~~electronic~~ circuit ~~further~~ comprises

a first ~~set of an~~ encoding means for encoding the output data into a first encoded output data,

a storage element for retrievably storing the first encoded output data,

a corresponding first decoding means, arranged for ~~encoding output data before storing the first output data in the storage element and~~ decoding the first encoded output data into said output data after retrieving the first encoded output data from the storage element~~, respectively~~, and

wherein the electronic circuit is arranged to dynamically control the activation of the first ~~set of~~ an encoding means and the [[a]] corresponding first decoding means.

6. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 5, wherein the storage circuit further comprises ~~comprising:~~

a second ~~set of an~~ encoding means for encoding the output data into a second encoded output data for storing in the storage element,

a corresponding second decoding means, arranged for ~~encoding output data before storing the first output data in the storage element and~~ decoding the second encoded output data into said output data after retrieving the second encoded output data from the storage element~~, respectively~~,

wherein the encoding of the first output data is different from the encoding of the second output data, and

wherein the electronic circuit is further arranged to dynamically select from among the first ~~one set of an~~ encoding means and its [[a]] corresponding first decoding means and the second ~~set of an~~ encoding means and its [[a]] corresponding second decoding means, for encoding and decoding of the output data.

7. (Currently Amended) The ~~An~~ electronic circuit of ~~according to~~ claim 6, further comprising a timing circuit ~~arranged~~ to determine the points in time at which the electronic circuit selects one from among the first and second ~~set of~~ encoding means and corresponding first and second decoding means~~, of a set comprising at least the first set of an encoding means and a corresponding decoding means and the second set of encoding means and a corresponding decoding means~~..

8. (Currently Amended ) The ~~An~~ electronic circuit of ~~according to~~ claim 5, wherein the combinatorial logical circuit comprises:

a first combinatorial logical circuit, having an input, arranged to perform a first set of logical operations on input data at the input and to produce a corresponding output data, the output data having a given functional relation to the input data, and ~~characterized in that the set of combinatorial logical circuits further comprises at least~~

a second combinatorial logical circuit, having an input, arranged to perform a second set of logical operations on ~~the same~~ input data at said input and to produce output data, the output data having a ~~an identical~~ functional relation to the input data identical to the given functional relation,

wherein the first set of logical operations is different from the second set of logical operations, and

a selector for receiving a given input data and ~~wherein the electronic circuit is arranged to~~ dynamically selecting from among the first ~~one~~ combinatorial logical circuit and the second combinatorial logical circuit ~~of the set of combinatorial logical circuits~~ for performing logical operations on the given ~~the~~ input data and producing output data, and

wherein the selecting includes inputting the given input data to the input of the selected one of the first and second combinatorial logical circuits and outputting a selected output, the selected output being the output of the selected one of the first and second combinatorial logical circuits.

9. (Canceled)

10. (Currently Amended) A method of processing cryptographic data, comprising:

[[-]] using a set of logical operations for processing input data and producing output data,

[[-]] storing the output data in a storage element, wherein the storing ~~characterized in that the method further~~ comprises:

[[-]] encoding the output data into an encoded output data ~~before storing the output data in the storage element~~,

storing the encoded output data in the storage element,

retrieving the encoded output data from the storage element,

[[-]] decoding the encoded output data retrieved ~~after retrieving~~ from the storage element, and

dynamically controlling the encoding of the output data into an encoded output data and the corresponding decoding of the encoded output data retrieved from the storage element.

11. (Previously Presented) A cryptographic device comprising an electronic circuit according to claim 1.

12. (New) The electronic circuit of claim 1, wherein the selector includes:

a first mask circuit for selectively masking and not masking, based on the signal, the given input data for input to the first combinatorial logical circuit, and

a second mask circuit for selectively masking and not masking, based on the signal, the given input data for input to the second combinatorial logical circuit.

13. (New) The electronic circuit of claim 8, wherein the selector includes:

a first mask circuit to selectively mask and not mask, based on the signal, the given input data and to input the selected masked and not masked given input data to the first combinatorial logical circuit, and

a second mask circuit to selectively mask and not mask, based on the signal, to input the selected masked and not masked given input data to the second combinatorial logical circuit.

14. (New) The electronic circuit of claim 13,

wherein the first mask circuit includes an AND mask configured to mask and to not mask the given input data by inputting to the first combinatorial logical circuit a selection between all zeros and the given input data, respectively and

wherein the second mask circuit includes an AND mask configured to mask and to not mask the given input data by inputting to the second

combinatorial logical circuit a selection between all zeros and the given input data, respectively.

15. (New) The electronic circuit of claim 1, wherein the selector includes an OR merger circuit to receive the output of the first combinatorial logical circuit and to receive the output of the second combinatorial logic circuit, and to output, as the selected output, a logical OR of the output of the first combinatorial logical circuit and the output of the second combinatorial logic circuit.

16. (New) A method of processing cryptographic data, comprising:

generating a mode signal having one of a given plurality of states;

receiving a given input data and generating a cryptographic processed data output, said generating including:

generating a first input data, wherein the first input data is a selected one of a mask of the given input data and a not mask of the given data, the selection based on the state of the mode signal;

generating a second input data, wherein the second input data is the other of the mask of the given input data and the not mask of the given data,

performing a first set of logical operations on the first input data to generate a first output data, the first set of logical operations embodying a given input-output function,

performing a second set of logical operations on the second input data to generate a second output data, the second set of logical operations being different than the first set of logical operations and the second set of logical operations embodying the same given input-output function, and

merging the first output data and the second output data to generate the cryptographic data output;

repeating said generating a mode signal to have a different one of the given plurality of states; and

repeating said receiving a given input data and generating a cryptographic processed data output.